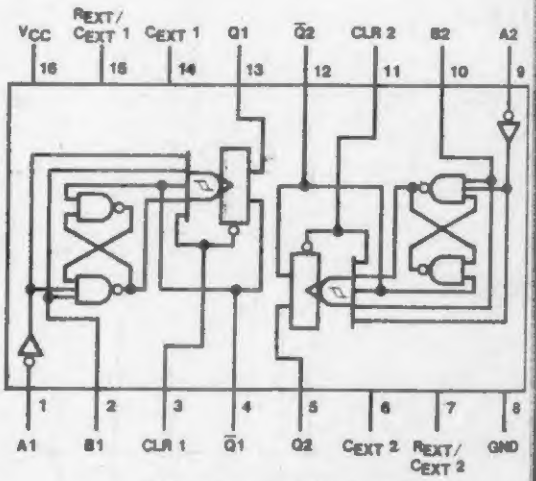
221 Dual One Shots with Schmitt-Trigger Inputs

Truth Table

Inputs			Outputs	
Clear	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎍
H	↓	H	⎍	⎍
↑	L	H	⎍	⎍

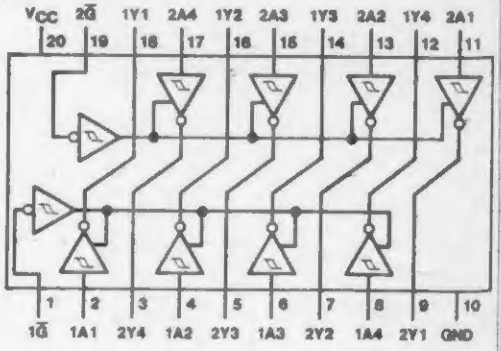


54LS221 (J,W); 74LS221 (N)

See page 5-44

Octal Buffers/Line Drivers/Line Receivers

240 Inverted TRI-STATE® Outputs

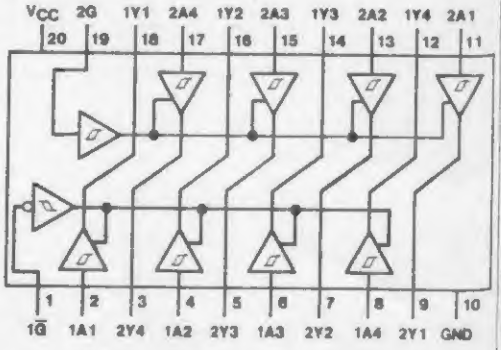


54LS240 (J) 74LS240 (N)
54S240 (J) 74S240 (N)

See page 5-53

Octal Buffers/Line Drivers/Line Receivers

241 Noninverted TRI-STATE Outputs



54LS241 (J) 74LS241 (N)
54S241 (J) 74S241 (N)

See page 5-53

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Conditions			DM54/74 121 Min	DM54/74 121 Typ (1)	DM54/74 121 Max	DM54/74 LS221 Min	DM54/74 LS221 Typ (1)	DM54/74 LS221 Max	Units
V_{T+}	Positive-Going Threshold Voltage at A Input	V_{CC} = Min				1.4	2		1.0	2	V
V_{T-}	Negative-Going Threshold Voltage at A Input	V_{CC} = Min		DM54	0.8	1.4		0.8	1.0		V
				DM74	0.8	1.4		0.8	1.0		
V_{T+}	Positive-Going Threshold Voltage at B Input	V_{CC} = Min				1.55	2		1.0	2	V
V_{T-}	Negative-Going Threshold Voltage at B Input	V_{CC} = Min		DM54	0.8	1.35		0.8	0.9		V
				DM74	0.8	1.35		0.8	0.9		
V_I	Input Clamp Voltage	V_{CC} = Min	I_I = −12 mA				−1.5				V
			I_I = −18 mA							−1.5	
I_{OH}	High Level Output Current						−400			−400	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = −400 μA		DM54	2.4	3.4		2.5	3.4		V
				DM74	2.4	3.4		2.7	3.4		
I_{OL}	Low Level Output Current			DM54			16			4	mA
				DM74			16			8	
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 4 mA						0.25	0.4	V
			I_{OL} = 8 mA	DM74					0.35	0.5	
			I_{OL} = 16 mA			0.2	0.4				
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5 V				1				mA
			V_I = 7 V							0.1	
I_{IH}	High Level Input Current	V_{CC} = Max	V_O = 2.4 V	A1 or A2			40				μA
				B			80				
			V_I = 2.7 V	All						20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4 V		A1 or A2			−1.6			−.4	mA
				B			−3.2			−.8	
				Clear			N/A			−0.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (2)		DM54	−20		−55	−20		−100	mA
				DM74	−18		−55	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max		Quiescent		13	25		4.7	11	mA
				Triggered		23	40		19	27	

Note 1: All typical values are V_{CC} = 5 V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and for DM54LS221/DM74LS221, duration of short circuit should not exceed one second.

Switching Characteristics at V_{CC} = 5 V, T_A = 25°C

	Parameter	From (Input)	To (Output)	DM54/74 121 Conditions	DM54/74 121 Min	DM54/74 121 Typ	DM54/74 121 Max	DM54LS/74LS LS221 Conditions	DM54LS/74LS LS221 Min	DM54LS/74LS LS221 Typ	DM54LS/74LS LS221 Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A1 or A2	Q	C_{EXT} = 80 pF, R_{INT} to V_{CC}		45	70	C_{EXT} = 80 pF, R_{EXT} = 2 kΩ		45	70	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	B	Q			35	55			35	55	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Clear	$\overline{Q}$			45	65			45	65	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A1 or A2	$\overline{Q}$			50	80			50	80	ns

Switching Characteristics at V_{CC} = 5 V, T_A = 25°C

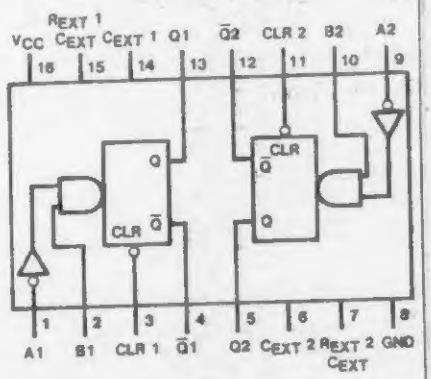
Parameter			From (Input)	To (Output)	DM54/74 121 Conditions		Min	Typ	Max	DM54LS/74LS LS221 Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		A1 or A2	Q	C_L = 15 pF, R_L = 400 Ω	C_{EXT} = 80 pF, R_{INT} to V_{CC}		45	70	C_L = 15 pF, R_L = 2 kΩ	C_{EXT} = 80 pF, R_{EXT} = 2 kΩ		45	70	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		B	Q				35	55				35	55	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Clear	$\overline{Q}$					N/A				45	65	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		A1 or A2	$\overline{Q}$				50	80				50	80	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		B	$\overline{Q}$				40	65				40	65	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Clear	Q					N/A				40	55	ns
$t_{W(OUT)}$	Output Pulse Width	Internal Timing Resistor (1)	A1, A2 or B	Q or $\overline{Q}$		C_{EXT} = 80 pF, R_{INT} to V_{CC}	70	110	150		C_{EXT} = 80 pF, R_{EXT} = 2 kΩ	70	120	150	ns
		Zero-Timing Capacitance				C_{EXT} = 0, R_{INT} to V_{CC}		30	50		C_{EXT} = 0, R_{EXT} = 2 kΩ	20	47	70	
		External Timing Resistor				C_{EXT} = 100 pF, R_{EXT} = 10 kΩ	600	700	800		C_{EXT} = 100 pF, R_{EXT} = 10 kΩ	600	670	750	
						C_{EXT} = 1 μF, R_{EXT} = 10 kΩ	6	7	8		C_{EXT} = 1 μF, R_{EXT} = 10 kΩ	6	6.7	7.5	ms
$t_{W(IN)}$	Input Pulse Width						50					40			ns
$t_{W(CLEAR)}$	Clear Pulse Width						N/A					40			ns
dv/dt	Rate of Rise or Fall of Input Pulse	Schmitt Input, B					1					1			V/s
		Logic Input, A					1					1			V/μs
R_{EXT}	External Timing Resistance					DM54	1.4		30		DM54	1.4		70	kΩ
						DM74	1.4		40		DM74	1.4		100	
C_{EXT}	External Timing Capacitance						0		1000			0		1000	μF
t_{SETUP}	Clear-Inactive State Setup Time								N/A			15			ns
	Duty Cycle					R_T = 2 kΩ			67		R_T = 2 kΩ			67	%
						R_T = Max R_{EXT}			90		R_T = Max R_T			90	

Note 1: Use of internal timing resistor applies to DM54/74121 only.

123 Dual Retriggerable One Shots with Clear

Truth Table
123, L123A

Inputs			Outputs	
A	B	CLR	Q	$\overline{Q}$
H	X	H	L	H
X	L	H	L	H
L	↑	H	⎍	⎍
↓	H	H	⎍	⎍
X	X	L	L	H

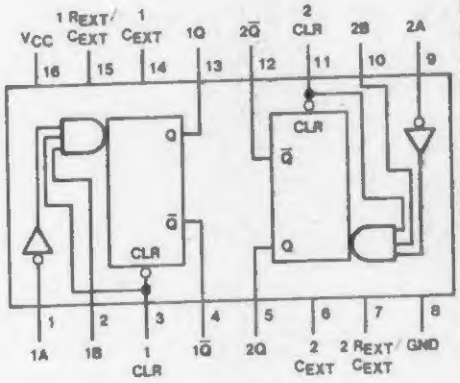


54123 (J,W)
54L123A (J,W)

74123 (N)
74L123A (N)

Truth Table
LS123

Inputs			Outputs	
Clear	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎍
H	↓	H	⎍	⎍
↑	L	H	⎍	⎍



54LS123 (J,W); 74LS123 (N)

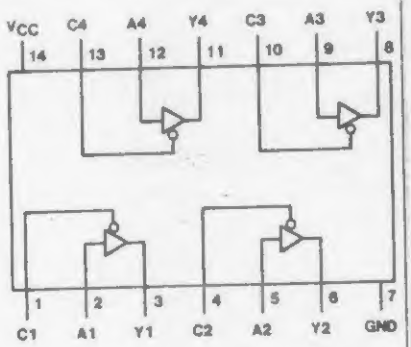
See page 5-46

125 TRI-STATE® Quad Buffers

Truth Table

Inputs		Output
A	C	Y
H	L	H
L	L	L
X	H	Hi-Z

Y = A



54125 (J,W)
54LS125A (J,W)

74125 (N)
74LS125A (N)

See page 5-48

Notes: ⎍ = one high-level pulse. ⎍ = one low-level pulse.
An external timing capacitor may be connected between C_{EXT} and R_{EXT}/C_{EXT} (positive).
For accurate repeatable pulse widths, connect an external resistor between R_{EXT}/C_{EXT} and V_{CC}.
To obtain variable pulse widths, connect external variable resistance between R_{EXT}/C_{EXT} and V_{CC}.

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Conditions			DM54/74 123			DM54/74 L123A			DM54/74 LS122, LS123			Units
					Min	Typ (1)	Max	Min	Typ (1)	Max	Min	Typ (1)	Max	
V_{IH}	High Level Input Voltage				2			2			2			V
V_{IL}	Low Level Input Voltage			DM54			0.8			0.7			0.8	V
				DM74			0.8			0.8			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min	I_I = −12 mA				−1.5			N/A				V
			I_I = −18 mA							N/A			−1.5	
I_{OH}	High Level Output Current						−800			−200			−400 [2]	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max (3)		DM54	2.4	3.4		2.4	3.4		2.5 [2]	3.4 [2]		V
				DM74	2.4	3.4		2.4	3.4		2.7 [2]	3.4 [2]		
I_{OL}	Low Level Output Current			DM54			16			2.0			4 [2]	mA
				DM74			16			3.6			8 [2]	
V_{OL}	Low Level Output Voltage	V_{CC} = Min (3)	I_{OL} = Max	DM54		0.2	0.4		0.22	0.3		0.25	0.4	V
				DM74		0.2	0.4			0.4		0.35	0.5	
			I_{OL} = 4 mA	DM74								0.25	0.4	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5 V				1			0.1				mA
			V_I = 7 V										0.1	
I_{IH}	High Level Input Current	Data Inputs	V_{CC} = Max	V_I = 2.4 V			40			10				μA
				V_I = 2.7 V									20 [3]	
		Clear Input		V_I = 2.4 V			80			10				
				V_I = 2.7 V									20 [3]	
I_{IL}	Low Level Input Current	Data Inputs	V_{CC} = Max, V_I = 0.4 V				−1.6			−0.18			−0.4	mA
		Clear Input					−1.6			−0.18			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (2) (3)			−10		−40	−2.5		−12	−20		−100 [2]	mA
I_{CC}	Supply Current (Quiescent or Triggered)	V_{CC} = Max (4) (5) (6)		LS122								6	11	mA
				Others		46	66		5	7.5		12	20	

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

Parameter		From (Input)	To (Output)	DM54/74 123				DM54/74 L123A				DM54/74 LS122, LS123				Units
				Conditions	Min	Typ	Max	Conditions	Min	Typ	Max	Conditions	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A	Q			22	33			120	175			22	33	ns
		B				19	28			86	135			29	44	
t_{PHL}	Propagation Delay Time,	A				30	40			120	180			30	45	

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

Parameter			From (Input)	To (Output)	DM54/74 123 Conditions	123 Min	123 Typ	123 Max	DM54/74 L123A Conditions	L123A Min	L123A Typ	L123A Max	DM54/74 LS122, LS123 Conditions	LS122, LS123 Min	LS122, LS123 Typ	LS122, LS123 Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		A	Q	C_{EXT} = 0, R_{EXT} = 5 kΩ, C_L = 15 pF, R_L = 400 Ω		22	33	C_{EXT} = 0, R_{EXT} = 32 kΩ, C_L = 50 pF, R_L = 4 kΩ		120	175	C_{EXT} = 0, R_{EXT} = 5 kΩ, C_L = 15 pF, R_L = 2 kΩ		22	33	ns
			B				19	28			86	135			29	44	
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		A	$\overline{Q}$			30	40			120	180			30	45	ns
			B				27	36			86	135			37	56	
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Clear	Q			18	27			45	85			18	27	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output			$\overline{Q}$			30	40			95	140			30	45	
$t_{WQ(MIN)}$	Minimum Width of Pulse at Output Q		A or B	Q			45	65			220	330			116	200	ns
t_{WQ}	Width of Pulse at Output Q		A or B	Q	C_{EXT} = 1000 pF, R_{EXT} = 10 kΩ, C_L = 15 pF, R_L = 400 Ω	3.08	3.42	3.76	C_{EXT} = 1000 pF, R_{EXT} = 100 kΩ, C_L = 50 pF, R_L = 4 kΩ	30.6	34.0	37.4	C_{EXT} = 1000 pF, R_{EXT} = 10 kΩ, C_L = 15 pF, R_L = 2 kΩ	4	4.5	5	μs
t_W	Pulse Width	A or B Inputs High				40				130				40			ns
		A or B Inputs Low				40				130				40			
		Clear Low				40				130				40			
R_{EXT}	External Timing Resistance		DM54			5		25		5		200		5		180	kΩ
			DM74			5		50		5		400		5		260	
C_{EXT}	External Capacitance					No Restriction				No Restriction				No Restriction			
C_{WIRE}	Wiring Capacitance at R_{EXT}/C_{EXT} Terminal		DM54					50				40				50	pF
			DM74					50				60				50	

Note 1: All typical values are at V_{CC} = 5 V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and for DM54LS/74LS duration of short circuit should not exceed one second.

Note 3: Ground R_{EXT}/C_{EXT} and input A, apply 2.4 V to the B input to measure the following: V_{OH} or I_{OS} at the Q output or V_{OL} at the $\overline{Q}$ output.

Note 4: Quiescent I_{CC} is measured (after clearing) with 2.4 V applied to all clear and A inputs, B inputs grounded, all outputs open, C_{EXT} = 0.02 μF, and R_{EXT} = 25 kΩ.

Note 5: I_{CC} is measured in the triggered state with 2.4 V applied to all clear and B inputs, A inputs grounded, all outputs open, C_{EXT} = 0.02 μF, and R_{EXT} = 25 kΩ.

Note 6: With all outputs open and 4.5 V applied to all data and clear inputs, t_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock (LS122, LS123).

TMS 9914 GENERAL PURPOSE INTERFACE BUS ADAPTER

990/9900 FAMILY MICROCOMPUTER COMPONENTS

- IEEE Std. 488-1975 Compatible
- Source and Acceptor Handshake
- Complete Talker and Listener Functions with Extended Addressing
- Controller and System Controller Capability
- Service Request
- Remote and Local with Lockout
- Serial and Parallel Polling
- Device Clear
- Device Trigger
- Compatible with TMS 9911 DMA Controller
- Single +5 V Power Supply
- Interfaces directly to SN75160/1/2 Transceivers

DESCRIPTION

The TMS 9914 General Purpose Interface Bus Adapter is a microprocessor controlled versatile device which enables the designer to implement all of the functions or a subset described in the IEEE Std. 488-1975. Using this standard, a variety of instruments can be interconnected and remotely or automatically programmed and controlled. The TMS 9914 is fabricated with N-channel silicon-gate technology and is completely TTL compatible on all inputs and outputs including the power supply (+5 V). It needs a single phase clock (nominally 5 MHz) which may be independent of the microprocessor system clock and, therefore, it can easily be interfaced with most microprocessors. The general purpose interface bus adapter (GPIBA) performs the majority of the functions contained in IEEE STd. 488-1975 and is versatile enough to allow software implementation of those sections not directly implemented in hardware.

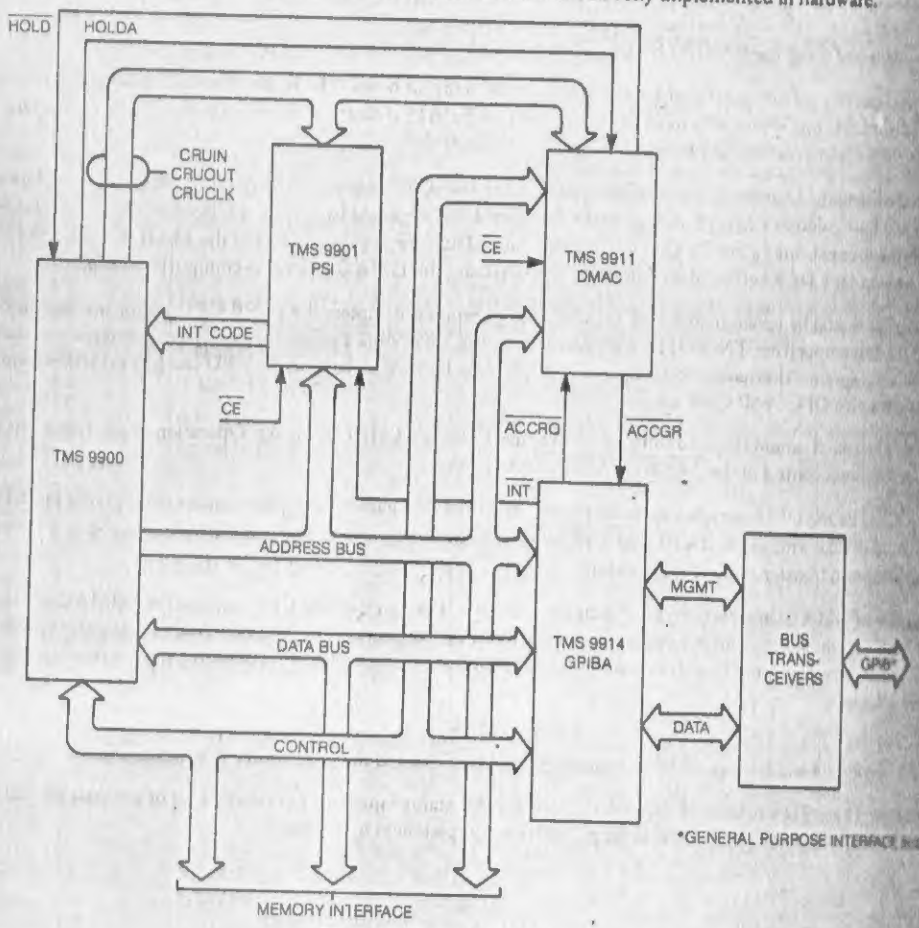


Figure 1. Typical System Interconnect

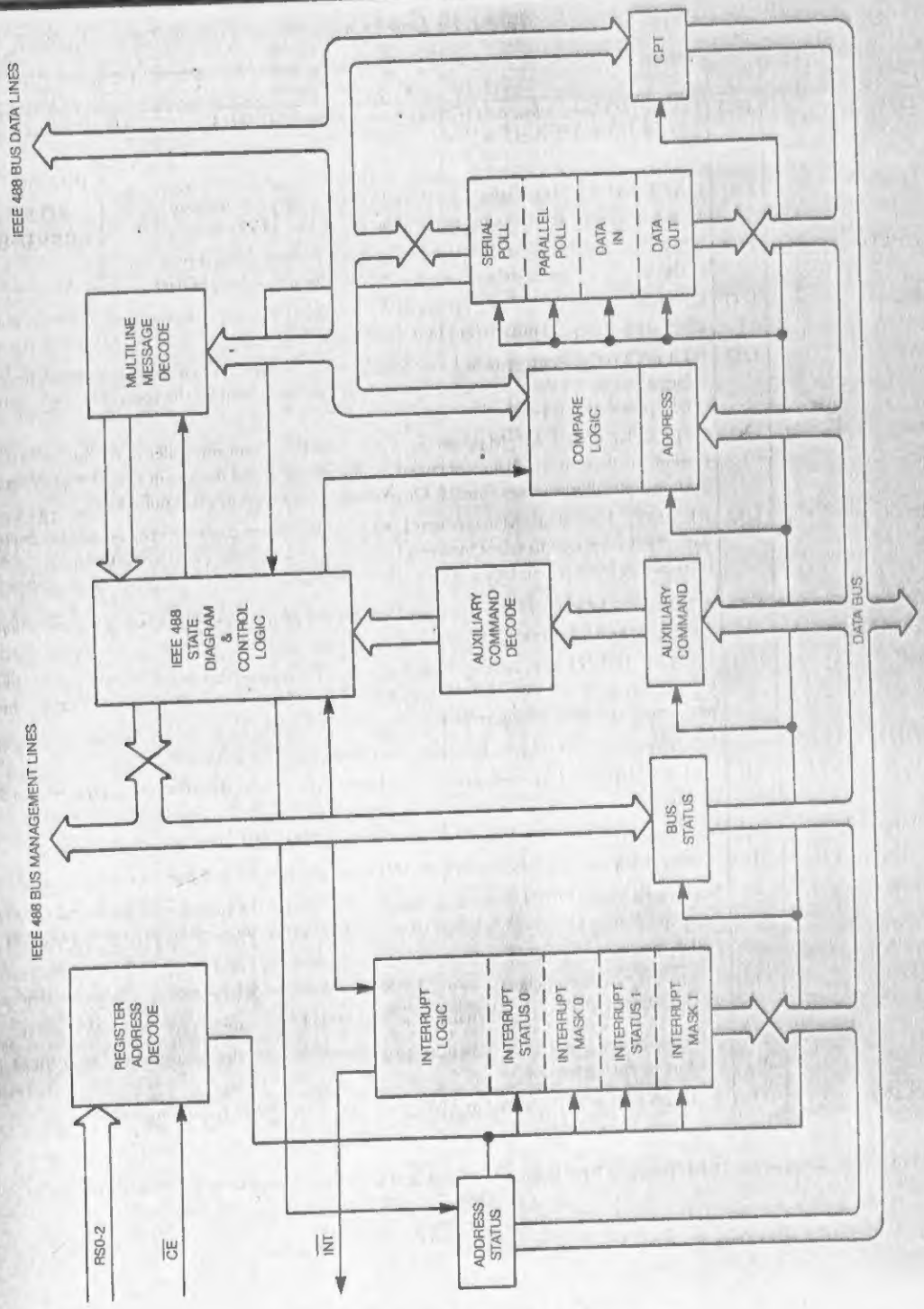


Figure 2. TMS 9914 Simplified Block Diagram

TMS 9914 GENERAL PURPOSE INTERFACE BUS ADAPTER

Table 1. Pin Description

Name	*I/O*	*Description*
DI01 through DI08	I/O	DATA I/O lines: allow data transfer between the TMS 9914 and the IEEE 488 data bus.
DAV	I/O	DATA VALID: Handshake Line. Sent by source device to indicate to acceptors that there is valid data on the IEEE bus data lines.
NRFD	I/O	NOT READY FOR DATA: Handshake Line. Sent by the acceptor to the source device to indicate when it is ready for a new byte of data.
NDAC	I/O	DATA NOT ACCEPTED: Handshake Line. Sent by acceptor to source device to indicate when it has accepted the current byte on the data bus.
ATN	I/O	ATTENTION: Management Line. Sent by the controller. When ATN is asserted, the information on the data lines is interpreted as commands, sent by the controller . . . When ATN is false, the data lines carry data.
IFC	I/O	INTERFACE CLEAR. Management Line. Sent by system controller to set the interface system, portions of which are contained in all interconnected devices in a known quiescent state. System controller assumes control. Open drain output with internal pullup.
REN	I/O	REMOTE ENABLE: Management Line. Sent by system controller and is used in conjunction with other messages to select between two alternate sources of programming data, e.g. via interface or front panel. Open drain output with internal pullup.
SRQ	I/O	SERVICE REQUEST: Management Line. Issued by a device on the bus to the controller to indicate a need for service.
EOI	I/O	END OR IDENTIFY: Management Line. If ATN is false, this signal is sent by the "talker" to indicate the end of a multiple byte transfer. If sent by the controller with ATN true, this will perform the parallel polling sequence.
$\overline{\text{CONTROLLER}}$	O	Bus transceiver control line. Indicates that the device is the controller.
TE	O	TALK ENABLE: Bus transceiver control line. Indicates the direction of data transfer on the data bus.
D0 through D7	I/O	Data I/O lines that allow transfer of data between TMS 9914 and the microprocessor.
RS0 through RS2	I	Address lines through which the TMS 9914 registers can be accessed by the microprocessor.
DBIN	I	When true (high) DBIN indicates to the TMS 9914 that the microprocessor is about to read from one of its registers. When false, that the microprocessor is about to write to one of its registers.
$\overline{\text{WE}}$	I	$\overline{\text{WRITE ENABLE}}$: indicates to the TMS 9914 that one of its registers is being written to.
$\overline{\text{CE}}$	I	$\overline{\text{CHIP ENABLE}}$: selects and enables the TMS 9914 for an microprocessor data transfer.
$\overline{\text{INT}}$	O	$\overline{\text{INT}}$: Open drain output. Sent to microprocessor to indicate the occurrence of an event on the bus requiring service.
$\overline{\text{ACCRQ}}$	O	$\overline{\text{ACCESS REQUEST}}$: Signal to TMS 9911 DMA controller requesting DMA.

PIN OUTS TO BE ASSIGNED

NOTE: The names of the IEEE bus lines have been maintained, and are therefore negative logic signals.

Table 3. Remote Multiple Message Coding

		DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1		Note
Addressed Command Group	ACG	X	0	0	0	X	X	X	X	AC	
Device Clear	DCL	X	0	0	1	0	1	0	0	UC	
Group Execute Trigger	GET	X	0	0	0	1	0	0	0	AC	
Go To Local	GTL	X	0	0	0	0	0	0	1	AC	
Listen Address Group	LAG	X	0	1	X	X	X	X	X	AD	
Local Lock Out	LLO	X	0	0	1	0	0	0	1	UC	
My Listen Address	MLA	X	0	1	L	L	L	L	L	AD	1
My Talk Address	MTA	X	1	0	T	T	T	T	T	AD	2
My Secondary Address	MSA	X	1	1	S	S	S	S	S	SE	3, 4
Other Secondary Address	OSA									SE	4, 5
Other Talk Address	OTA				TAG + MTA					AD	
Primary Command Group	PCG									–	6
Parallel Poll Configure	PPC	X	0	0	0	0	1	0	1	AC	7
Parallel Poll Enable	PPE	X	1	1	0	S	P	P	P	SE	8, 9
Parallel Poll Disable	PPD	X	1	1	1	D	D	D	D	SE	8, 10
Parallel Poll Unconfigure	PPU	X	0	0	1	0	1	0	1	UC	11
Secondary Command Group	SCG	X	1	1	X	X	X	X	X	SE	
Selected Device Clear	SDC	X	0	0	0	0	1	0	0	AC	
Serial Poll Disable	SPD	X	0	0	1	1	0	0	1	UC	
Serial Poll Enable	SPE	X	0	0	1	1	0	0	0	UC	
Take Control	TCT	X	0	0	0	1	0	0	1	AC	12
Talk Address Group	TAG	X	1	0	X	X	X	X	X	AD	
Universal Command Group	UCG	X	0	0	1	X	X	X	X	UC	
Unlisten	UNL	X	0	1	1	1	1	1	1	AD	
Untalk	UNT	X	1	0	1	1	1	1	1	AD	

Symbols: AC – Addressed Command
AD – Address (Talk or Listen)
UC – Universal Command
SE – Secondary (Command or Address)
0 – Logical Zero (high level on IEEE Bus; Low level within 9914).
1 – Logical One (Low level on IEEE Bus; High level within 9914).
X – Don't Care (received message)
X – Must Not Drive (transmitted message)

Notes to Table 3:

1. L L L L L: Represents the coding for the device listen address.
2. T T T T T: Represents the coding for the device talk address.
3. S S S S S: Represents the coding for the device secondary address.
4. Secondary addresses will be handled via address pass through.
5. OSA will be handled as an invalid secondary address pass through by the MPU.
6. PCG = ACG ∨ UCG ∨ LAG ∨ TAG
7. PPC will be handled in software by the MPU via Unrecognized Address Command Group pass through.
8. PPE, PPD will be handled via pass through next secondary feature.
9. S P P P represents the sense and bit for remote configurable parallel poll.
10. D D D D specify don't care bits that must be sent all zeroes, but need not be decoded by receiving device.
11. PPU is handled via Unrecognized Universal Command Group pass through.
12. TCT will be handled via Unrecognized Addressed Command Group pass through. However, in this case, the device must be in TADS before the pass through will occur.

Interrupt Status Registers 0 and 1

INT0	INT1	BI	BO	END	SPAS	RLC	MAC
GET	UUCG	UACG	APT	DCAS	MA	SRQ	IFC

INT0	An interrupt occurred in register 0
INT1	An interrupt occurred in register 1
BI	A byte has been received
BO	A byte has been output
END	An EOI occurred with ATN false
SPAS	Serial Poll Active State has occurred with rsv set in the Serial Poll register
RLC	A REMOTE/LOCAL change has occurred
MAC	An address change has occurred
GET	A Group Execute Trigger has occurred
UUCG	An Undefined Universal Command has been received
UACG	An Undefined Addressed Command has been received. This bit will also be set on receipt of a secondary command when the pts feature in the Auxiliary Command register is utilized.
APT	A secondary address has occurred
DCAS	Device Clear Active State has occurred
MA	My Address (MLAVMTA)·$\overline{SPSM}$
SRQ	A Service Request has been received
IFC	An IFC has been received

INT0 is the logical OR of each bit of Interrupt Status Register 0 ANDed with the respective bit of Interrupt Mask Register 0. INT1 is the same but applies to Interrupt Mask and Status Register 1. Reading either Interrupt Status Register will also clear it. The INT line will be cleared only when the interrupt status register which caused the interrupt is read.

Interrupt Mask Registers 0 and 1

		BI	BO	END	IFC	RLC	MAC
GET	UUCG	UACG	APT	DCAS	MA	SRQ	SPAS

The Interrupt Mask Registers 0 and 1 correspond to the Interrupt Status Registers 0 and 1 respectively, with the exception of INT0 and INT1.

Address Status Register

REM	LLO	ATN	LPAS	TPAS	LADS ∨ LACS	TADS ∨ TACS	ulpa

The Address Status Register is used to convey the addressed state of the talker/listener and the remote/local and local lockout condition. This information is derived from the TMS 9914 internal logic states at the time of reading. The ninth bit is used for dual addressing and indicates the state of the LSB of the bus at last primary addressed time.

Bus Status Register

ATN	DAV	NDAC	NRFD	EOI	SRQ	IFC	REN

The Bus Status Register allows the microprocessor to obtain the current status of the IEEE 488 Bus Management Lines.

Auxiliary Command Register

C/S	X	X	f4	f3	f2	f1	f0

The Auxiliary Command Register allows control of additional features on chip and provides a means of inputting some of the local messages to the interface functions. Table 4 lists these messages and commands. If C/S = 1, the feature will be set and if C/S = 0, the feature will be cleared. If C/S = NA, it should be sent as zero.

Table 4. Auxiliary Commands

Function	*Mnemonic*	*C/S*	*f4*	*f3*	*f2*	*f1*	*f0*
Chip Reset	rst	0/1	0	0	0	0	0
Release ACDS holdoff	dacr	0/1	0	0	0	0	1
Release RFD holdoff	rhfd	NA	0	0	0	1	0
Holdoff on all data	hdfa	0/1	0	0	0	1	1
Holdoff on EOI only	hdfe	0/1	0	0	1	0	0
Set new byte available false	nbaf	NA	0	0	1	0	1
Force group execute trigger	fget	0/1	0	0	1	1	0
Return to local	rtl	0/1	0	0	1	1	1
Return to local immediate	rtli	0	0	0	1	1	1
Send EOI with next byte	feoi	NA	0	1	0	0	0
Listen only	lon	0/1	0	1	0	0	1
Talk only	ton	0/1	0	1	0	1	0
Take control synchronously	tcs	NA	0	1	1	0	0
Take control asynchronously	tca	NA	0	1	1	0	0
Go to standby	gts	NA	0	1	0	1	1
Request parallel poll	rpp	0/1	0	1	1	1	0
Send interface clear	sic	0/1	0	1	1	1	1
Send remote enable	sre	0/1	1	0	0	0	0
Request contol	rqc	NA	1	0	0	0	1
Release control	rlc	NA	1	0	0	1	0
Disable all interrupts	dai	0/1	1	0	0	1	1
Pass through next secondary	pts	NA	1	0	1	0	0
Set T1 delay	stdl	0/1	1	0	1	0	1

TMS 9914 GENERAL PURPOSE INTERFACE BUS ADAPTER

Address Register

edpa	dal	dat	A5	A4	A3	A2	A1

edpa enable dual primary addressing

dal disable the listen function

dat disable the talk function

A1 – A5 primary device address

The Address Switch Register corresponds to the Address Register. A power-up RESET or a rst command with C/S = 1 will leave the chip in a totally idle state. At this point, the Address Switch Register is read and the value is written into the Address Register. The reset condition is then cleared by sending rst with C/S = 0.

Serial Poll Register

S8	rsv	S6	S5	S4	S3	S2	S1

The Serial Poll register is used to establish the status byte that is sent out when the controller conducts a serial poll. Bits 1 through 6 and 8 contain status information, while bit 7, rsv, is used to enable the SRQ line and to indicate to the controller which device(s) was responsible for making a service request.

Command Pass Through Register

DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1

The Command Pass Through Register is used to pass through to the microprocessor any commands or secondary addresses that are not automatically handled in the TMS 9914.

Parallel Poll Register

PP8	PP7	PP6	PP5	PP4	PP3	PP2	PP1

This register contains the status bit that is output when the controller conducts a parallel poll.

Data-In Register

DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1

The data-in register is used to move data from the interface bus when the chip is addressed as a listener. Upon receipt of a data byte, the chip will hold NRFD true until the microprocessor reads the data-in register, when NRFD will be set false automatically.

Data-Out Register

DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1

The data-out register is used to move data from the TMS 9914 onto the IEEE std 488-1975 data bus.

After sending a byte out on the bus, the device can take part in a new handshake only after a new byte is placed in the data-out register, when it will be able to send DAV true again.